GAMMA RAY EFFECTS ON FLASH MEMORY CELL ARRAYS

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Information stored in flash memories is physically represented by the absence or presence of charge on electrically isolated floating gates. Interaction of gamma rays with the insulators surrounding the floating gate produces effects that degrade the properties of memory cells, possibly leading to the corruption of the stored content. The cumulative nature of these effects is expressed through the total ionizing dose deposited by the gamma rays in the insulators surrounding the floating gate. Relying on both theory and experiment, we examine how the properties of cells in commercially available flash memories affect their sensitivity to gamma rays. Memory samples from several manufacturers, currently available on the market, can be compared with respect to data retention under gamma ray exposure.

Key words: flash memory, gamma rays, floating gate, total ionizing dose

INTRODUCTION

Flash memories have become a dominant type of non-volatile memory in many applications, some of which require electronic parts to operate in radiation environments. In recent years, even the applications that require rad-hard electronic components rely on commercially available chips, selected by detailed survey procedures.

The interaction of radiation with the insulators surrounding the floating gate (FG) degrades the properties of memory cells, possibly leading to the corruption of the stored content, performance impairment, or loss of functionality. The extent of the effects that gamma rays, X-rays or light charged particles (*e. g.* electrons and protons) traversing a flash memory cell array produce, depends primarily on the absorbed dose. These effects are consequently termed total ionizing dose (TID) effects. The functionality of flash memories begins to fail as TID accumulates [1-3]. Radiation-induced changes in the FG involve several different physical mechanisms which take place on different time scales, with different field and temperature dependencies. The overall radiation response of a flash memory cell array can be very complex. It has, therefore, been a practice to investigate the components of a flash memory individually. Many different investigators have studied different parts of the radiation response over a period of many years [4-9].

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We have investigated gamma ray effects on flash cell arrays by irradiating four flash memory models. The memories were produced by various manufacturers and are all currently commercially available. Results obtained from these experiments are interpreted in terms of the interaction of gamma rays with the memory cells' inner structure. The tested memory samples are also compared with respect to data retention after gamma ray exposure.

In addition to the TID effects, two other types of radiation effects encountered in integrated circuits are single event effects (SEE) produced by the passage of heavy ions and the displacement damage, which is more relevant for neutron and ion beam irradiation. These two kinds of radiation effects are not of interest when gamma ray exposure of flash memories is considered.

DESIGN AND OPERATION CHARACTERISTICS OF CURRENT FLASH MEMORIES

A flash memory cell is a MOS transistor with an additional insulated polysilicon layer, the so called floating gate (FG), interposed between the substrate (body) and the control gate (CG), as shown schematically in fig. 1. The interpoly dielectric between FG and CG is typically an oxide-nitride-oxide (ONO) structure, consisting of two layers of SiO_2 sandwiching a thin film of Si_3N_4. The function of the interpoly di-

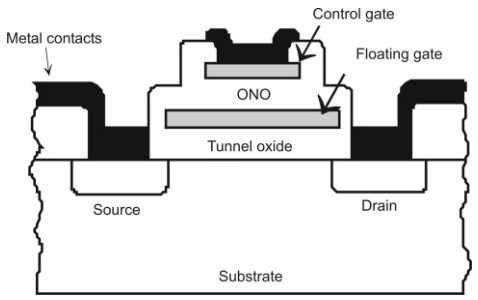

Figure 1. Lateral cross-section of a flash memory cell

electric is to minimize the leakage of the charge stored at the FG and, at the same time, to provide the best capacitive coupling between the floating and the control gate. The dielectric separating the FG and the substrate is called the tunnel oxide and is usually made of high-quality SiO_2 [10].

Charge stored on the floating gate determines the value of transistor threshold voltage, making the memory cell either "on" or "off" at readout. Figure 2 shows the drain current versus gate voltage for a FG transistor. The left curve corresponds to an "erased" state, with positive or no charge on the FG. The right curve corresponds to a "programmed" transistor with a net negative charge stored on the FG. When read with a bias CG voltage intermediate between the threshold voltages of the erased and the programmed state, an erased cell is "on" and conducts a significant amount of current, whereas a programmed one is "off" and draws little or no current [11].

Floating gate cells in the memory core form either NOR or NAND arrays, presented in fig. 3(a) and 3(b), respectively. NOR architecture utilizes channel hot electron programming, which consists of applying high voltages (~10 V) to both the drain and the CG, while the source and bulk (substrate) are kept at 0 V. With such biasing, a large current (0.3 to 1 mA) flows through the channel between the drain and the source. Some of the electrons from this current that scatter off

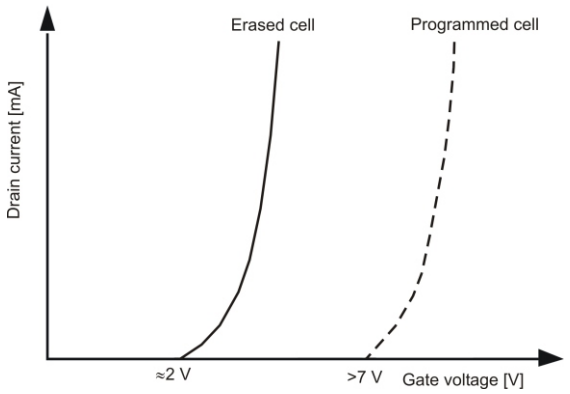

Figure 2. Flash cell's current-voltage characteristic (drain current *vs*. gate voltage) in the erased and programmed state

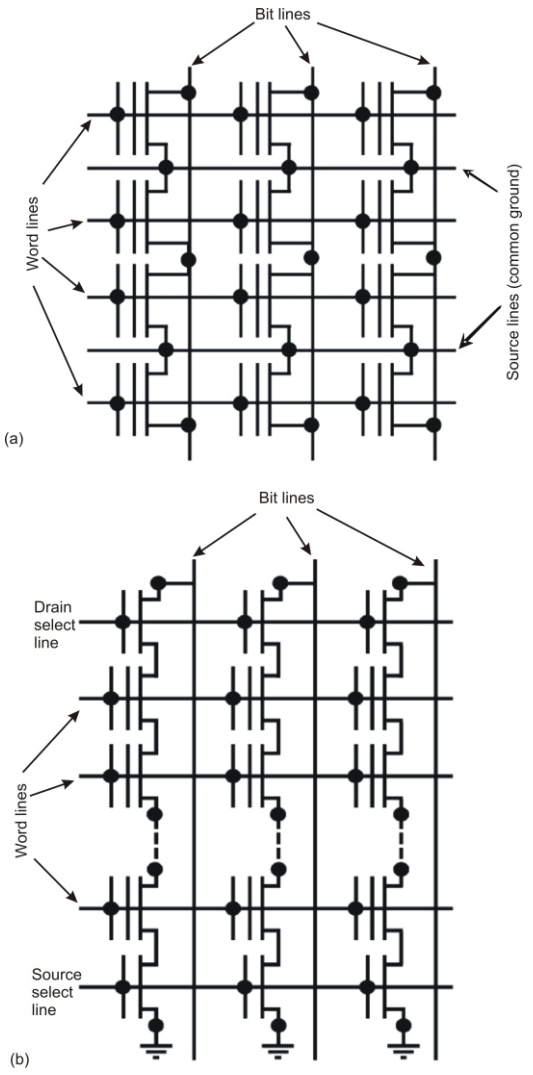

Figure 3. Flash memory cell array in (a) NOR and (b) NAND architecture

the crystal latice toward the FG have enough energy to overcome the substrate-to-insulator barrier (Si/SiO_2 barrier of 3.1eV), cross the insulator, and reach the FG. Voltage applied to the CG establishes a field accross the tunnel oxide that favors the injection. Hot electron injection is an inefficient method by which only about 0.001% of the channel current is directed to the FG. Memories with NAND architecture rely on a slower, but more efficient and better controlled programming process, based on cold electron tunneling. It consists of applying a high voltage (~20 V) to the CG, while the drain, source and bulk are grounded. Electrons from the substrate tunnel flow through the Si/SiO_2 potential barrier and cross the thin (~10 nm) tunnel oxide. Tunnel programming requires only a very small channel current (<1 nA), allowing many cells to be programmed at the same time [11].

While their programming mechanisms differ, both NOR and NAND devices use the tunneling of electrons from the FG to the substrate to erase cells.

The erase operation is performed on blocks of cells, by reverse biasing the cells' CGs with respect to the source (NOR) or the body (NAND).

In NOR architecture, each two neighbouring cells share a drain contact connected to the bit line (fig. 3(a). Since a drain contact has to be produced for every pair of cells and because hot electron programming poses a limit on the shortening of channel and gate length, NOR memories have lower packing densities than NAND devices. The NOR organization of cells enables fast random access at word level and is suited to read-mostly memories for code storage.

NAND memories have the smallest bit size in semiconductor industry, owing to the absence of a drain contact for each cell and there being no restriction on channel length imposed by the programming mechanism. In addition to the series arrangement of cells in strings (seen in fig. 3(b), multiple strings are connected to the same bit lines in parallel (not presented in fig. 3(b). Two additional transistors at the top and bottom of each string, connected to the so called drain and source select lines, respectively, serve to select a particular set of strings from this parallel configuration. The read operation is more complex in NAND than in NOR memories, because all unselected cells in the string containing the cell to be read must be turned "on", while only the selected cell is allowed to influence the current flow through the string. To achieve this, the gates of the unselected cells are biased at the so called "pass voltage", high enough to keep both programmed and erased cells "on". The gate of the cell to be read is biased at a "read voltage", higher only than the threshold voltage of a programmed cell. The first access to a page is slow, because of the time needed for the drain current to propagate through the whole string of cells. Further sequential access to the already selected strings is, however, much faster. This fact, along with the high packing density, makes NAND flash memories suited to large capacity data storage applications that require fast serial reads and writes (such as audio or video storage), and do not depend on random access [10-12].

EXPERIMENTAL SET-UP AND RESULTS

Commercial NAND devices typically do not guarantee 100% good bits, which poses a demand for on-chip error correction coding (ECC) circuitry. In NOR architecture, the manufacturer guarantees that each single bit is functional, so that no ECC has to be implemented. In some cases, however, an internal ECC transparent to the user may be present even in NOR devices. This is mainly the case with flash memories with multi-level cells. For our experiments, we have chosen to irradiate NOR memories from different manufacturers. The conclusions drawn from the analysis of experimental results are, however, valid for NAND flash memories as well, since they concern radiation effects occurring at the level of FG cells, regardless of the specific array architecture [11].

Four flash memory models were investigated, all with 512 kbit storage capacity: Numonyx M25P05-A (denoted Type 1 in this paper), Atmel AT25F512B (Type 2), SST SST25VF512 (Type 3), and Macronix MX25L5121E (Type 4). Type 1 memory had a TSSOP8 package, while the other three types were in 8-lead SOIC packages.

The tested memory chips were all programmed with a "checkerboard pattern" of alternating "on" and "off" cells before irradiation, with pins left floating during exposures. In this way, we have examined the influence of gamma ray exposure on the retention of the investigated memories, *i. e.* on their ability to preserve the stored information when there is no bias [13].

Irradiation was performed at the ^{60}Co irradiation unit in the Laboratory for Radiation Chemistry and Physics, Vinča Institute of Nuclear Sciences, Belgrade, Serbia. The radiation field at the unit is characterized by the absorbed dose rate values in air at various distances from the source. The dose absorbed by the memory samples was specified by changing the duration of irradiation and the position of the samples within the field. The absorbed dose in silicon was calculated from the absorbed dose in the air, by using appropriate mass energy-absorption coefficients for an average energy of ^{60}Co gamma rays equal to 1.25 MeV. All tests were performed at room temperature (25 ºC).

Five samples of each of the four memory types were irradiated at every absorbed dose level. The absorbed dose (total ionizing dose) ranged from 1 to 12 kGy, with an increment of 1 kGy. The results presented herein were obtained as mean values for each of the 5-sample batches. Type A measurement uncertainty associated with the results was about 10% for all batches.

Graphs in fig. 4 present the post-irradiation bit error percentage (*i. e.* the number of bit upsets relative to the total size of 512 kbits) versus the absorbed dose, for the four tested memory types. All four investigated memory models manifested a steady rise of the number of bit errors with dose, up to a dose of about 9 kGy, after which a saturation of the bit error percentage is observed (fig. 4). Type 2 memory demonstrated a somewhat more abrupt rise of the bit error count in the lower dose range, compared to the other three types, already saturating at 5 kGy. Type 1 memory reached the highest bit error percentage at maximum dose (65%), while the lowest number of bit errors was found in Type 4 memory (42% at 12 kGy). Type 3 memory showed the least saturation, suggesting that for this memory model, the bit error count might have risen further at doses above 12 kGy.

Graphs in fig. 5 show the results of room temperature annealing for the samples exposed to the highest

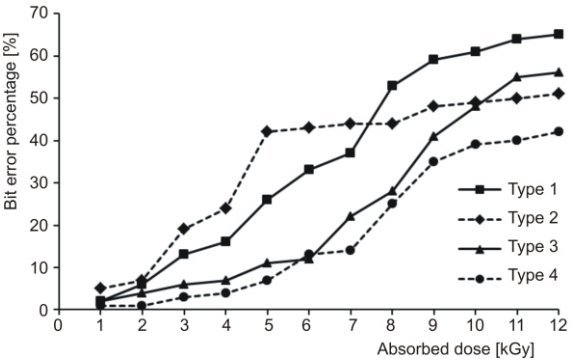

Figure 4. Recorder values of bit error percentage *vs*. the absorbed dose (total ionizing dose) in the four investigated flash memory types

dose of 12 kGy. The bit error percentage was monitored weekly, for a total duration of nine weeks. All four memory types exhibited a moderate recovery of the stored content, having between 17% (Type 4) and 32% (Type 2) of bit errors nine weeks after irradiation.

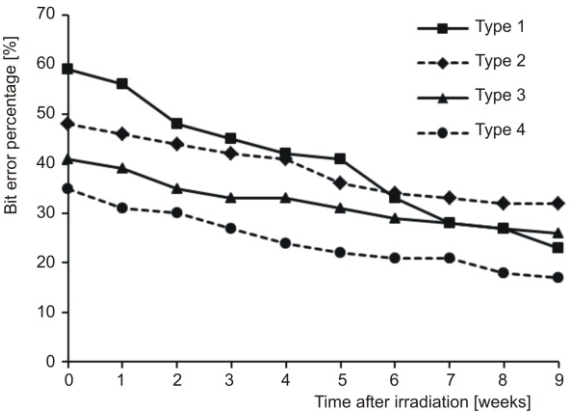

Figure 5. Room temperature annealing of the four tested flash memory types in the nine weeks following maximum dose (12 kGy) irradiation

ANALYSIS OF THE RESULTS

When passing through the oxides (tunnel and ONO), gamma rays create electron/hole pairs. If energetic enough, these secondary charged particles can produce additional electron/hole pairs. Generated electrons and holes can either recombine or be separated by the electric field present across the oxides, due to the charge stored in the FG and/or the work function differences between materials that constitute the memory cell [14-16].

The radiation-induced charge that evades recombination gets injected into the FG. In programmed cells, with electrons stored in the FG, the field in the surrounding oxides causes the injection of holes into the FG, which recombine the stored electrons and thereby decrease the cell's threshold voltage. The opposite holds true for erased cells with holes stored in the FG, in which the threshold voltage rises.

Another effect caused by gamma rays is the photoemission from the FG of charge carriers that get enough energy to overcome the potential barrier. The loss of electrons from the FG in programmed cells causes additional decrease of the threshold voltage, while in erased cells the removal of holes from the FG further increases the threshold voltage.

The third mechanism that could cause a flash memory cell's threshold voltage to change is the trapping of the charge in the tunnel oxide. This effect is typically small, because of the small thickness of tunnel oxides in present-day flash memories, but can be significant for post-irradiation annealing. The net sign of the trapped charge can be either + or ?, depending on weather electrons or holes predominantly occupy the trapping sites existing within the oxide and at FG/oxide and oxide/substrate interfaces. The trapping mechanism, therefore, gives rise to a state-dependent threshold voltage shift which can change over time, due to the tunnelling of electrons from the substrate to the trapping sites [17-21].

The net effect of radiation is such that the threshold voltage is shifted to lower values in "off" (programmed) cells and to higher values in "on" (erased) cells, meaning that both states are liable to perturbation. If the radiation-induced shift of the threshold voltage is large enough, it leads to an erroneous readout of the memory cell's logic state. Such erroneous readouts appear as bit errors (upsets) observed in experiments.

The fact that all tested memories exhibited a partial recovery during room temperature annealing suggests that the charge trapped within the tunnel oxide or at its interfaces gets compensated by the charge tunnelling from the substrate [22, 23].

CONCLUSIONS

The retention of four commercially available flash memory models after gamma ray exposure has been investigated. The rise of bit error percentage following the rise of the total ionizing dose is attributed to radiation-induced effects in both the tunnel oxide and the interpoly dielectric of the memory cells. A theoretical analysis of these effects indicates that the radiation-induced shift of the cells' threshold voltage leans toward lower values in programmed cells, as opposed to the higher values in the erased cells. This makes both cell states susceptible to perturbations that give rise to read errors observed in experiments. Bit error counts did not differ much among various memory models, meaning that the sensitivity to gamma ray exposure depends primarily on the dimensions of oxide

layers which are nearly equal for the four tested memory types, since they all belong to the same technology node. Partial room temperature annealing of radiation-induced bit errors has been observed in all four memories and is attributed to a gradual compensation of the charge trapped in the oxide by electrons tunnelling from the substrate.

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УТИЦАЈ ГАМА ЗРАЧЕЊА НА НИЗОВЕ ЋЕЛИЈА У ФЛЕШ МЕМОРИЈАМА

Подаци ускладиштени у флеш меморију физички су представљени одсуством или присуством наелектрисања на електрично изолованим пливајућим гејтовима. Интеракција гама зрака са изолаторима који окружују пливајући гејт ствара ефекте који погоршавају особине меморијских ћелија и могу да измене упамћен садржај. Кумулативна природа ових ефеката изражава се укупном дозом јонизације коју гама зраци депонују у изолаторима око пливајућег гејта. Ослањањем на теорију и експеримент, у овом раду је анализирана осетљивост комерцијално доступних флеш меморија на излагање гама зрацима, у зависности од карактеристика њихових ћелија. Узорци меморија више произвођача, тренутно заступљених на тржишту, упоређени су са становишта очувања података при озрачивању.

Кључне речи: флеш меморија, гама зраци, пливајући гејт, укупна јонизациона доза