

## ANNEALING OF RADIATION-INDUCED DEFECTS IN BURN-IN STRESSED POWER VDMOSFETs

by

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The annealing of radiation-induced defects in burn-in stressed *n*-channel power VDMOSFETs with thick gate oxides (100 and 120 nm) is analysed. In comparison with the previous spontaneous recovery, the changes of device electrical parameters observed during annealing are highlighted by the elevated temperature and voltage applied to the gate, and are more pronounced in devices with a 120 nm thick gate oxide. The threshold voltage of VDMOSFETs with a 100 nm thick gate oxide during annealing has an initially slow growth, but then increases rapidly and reaches the value higher than the pre-irradiation one (rebound effect). In the case of devices with a 120 nm thick gate oxide, the threshold voltage behaviour also consists of a slight initial increase followed by a rapid, but dilatory increase, with an obvious tendency to achieve the rebound. The changes of channel carrier mobility during annealing are similar in all samples: at first, it slowly and then rapidly declines, and after reaching the minimum it begins to increase. In the case of VDMOSFETs with a thicker gate oxide, these changes are much slower. The underlying changes in the densities of gate oxide-trapped charge and interface traps are also delayed in devices with a thicker gate oxide. All these phenomena occur with certain delay in burn-in stressed devices compared to unstressed ones. The leading role in the mechanisms responsible for the observed phenomena is attributed to hydrogen related species.

*Key words:* VDMOSFET, threshold voltage, channel carrier mobility, rebound effect, gate oxide charge, interface traps, latent interface trap buildup, burn-in

### INTRODUCTION

Because of the superior switching characteristics which provide reliable operation at frequencies higher than 100 kHz [1], power VDMOS (Vertical Double-Diffused MOS) transistors have become very attractive devices for high frequency switching power supply units used in medical, aircraft and military electronics, engine control systems, electronic systems in nuclear facilities, cosmic vehicles, *etc.* An important requirement for power VDMOSFETs assembled in electronic systems for application in a radiation environment (communication satellites, nuclear power plants, nuclear weapons and other military equipment) is high radiation tolerance. The knowing of radiation tolerance is important since during long-term missions of communication satellites the devices can accumulate significant overall dose depending on satellite or-

bits [2-4]. It was found that devices in low-Earth orbits can accumulate the total radiation dose of up to 100 Gy, while in a high orbits the dose can reach even  $10^4$  Gy [5].

It is well known that ionizing radiation leads to the formation of the positive charge in the gate oxide ( $N_{ot}$ ) and interface traps at the oxide-semiconductor interface ( $N_{it}$ ), which may cause changes in the threshold voltage ( $V_T$ ), reduction of carrier mobility ( $\mu$ ), current leakage increase, and breakdown voltage reduction in VDMOSFETs [6-8]. The decrease of  $V_T$  is the most serious problem in commercial *n*-channel VDMOSFETs, because it can change their functionality, leading to possible functional errors of the electronic system the transistors are assembled in. Even the radiation-hardened power VDMOSFETs may fail due to the degradation of  $\mu$  and changes of  $V_T$  [6].

Another important requirement for application in radiation environment is high reliability of power VDMOSFETs. It is achieved through the process of

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selection, by performing reliability screening for all delivered devices, thus reducing possible “infant mortality”. In the case of power MOSFETs, standard reliability screening includes “burn-in tests” (US MIL-STD 883, Test Method 1015), such as: high temperature reverse bias (HTRB), high temperature gate bias (HTGB) and high temperature storage life (HTSL) stresses [9]. However, HTGB stress was shown to affect the radiation response in MOS transistors [10], so the standard qualification testing for the application of MOSFETs in radiation environment was modified by imposing the requirement for radiation qualification testing after burn-in (US MIL-STD 883, Test Method 1019). The need for modified qualification testing has been confirmed by our recent results [11-13], which have shown that burn-in tests could have significant impact in the case of power VDMOSFETs as well, not only on their radiation response, but also on the annealing of radiation defects.

Gate oxide thickness is an important technological parameter having a significant impact on the electrical characteristics of MOS devices upon stress [14, 15]. A dependence of radiation-induced shift of  $V_T$  on the gate oxide thickness  $t$  was found to follow the power law  $t^n$  ( $n$  is between 1 and 3 [15], depending on processing history and electrical biasing effects). This is caused by the hydrogen released during the process of high temperature oxidation and incorporated into the oxide structure, breaking and/or weakening the original atomic bonds in the oxide and at the interface, and thus contributing to the increase in  $N_{ot}$  and  $N_{it}$  [16].

Hence, the response of power VDMOSFETs to different types of stress could vary depending on gate oxide thickness, so in this paper we present a detailed analysis of annealing effects on electrical parameters in irradiated VDMOSFETs with thick gate oxides subjected to pre-irradiation burn-in stress. The influence of gate oxide thickness on post-radiation annealing response will be discussed in terms of the mechanisms responsible for the observed changes in the densities of  $N_{ot}$  and  $N_{it}$ .

## EXPERIMENTAL RESULTS

The devices used were commercial  $n$ -channel power VDMOSFETs EFL1N10, manufactured by Ei-Semiconductors, Serbia, in standard Si-gate technology. 30 randomly taken devices with 100 nm thick gate oxide (batch A) and 30 randomly taken devices with a 120 nm thick gate oxide (batch B) were used. Devices from both batches were electrically characterized and divided into three groups of 10 samples each.

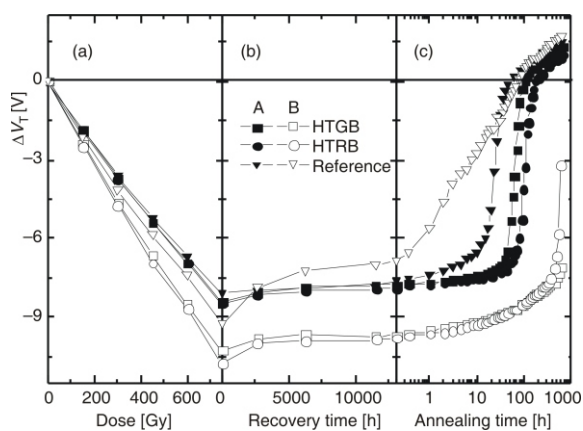
Devices from the first group were not subjected to pre-irradiation burn-in stressing and were used as a reference. The other two groups were stressed before irradiation: devices from the second group were subjected to HTRB stress, while devices from the third

group were subjected to HTGB stress. An 80 V positive dc bias was applied to the drain (gate and source terminals grounded) for HTRB stressing, whereas HTGB stress was performed by applying the 20 V positive dc bias to the gate, with drain and source terminals grounded. Both HTRB and HTGB stresses were carried out at 125 °C for 168 hours in a Heraeus HEP2 burn-in system. Electrical characterization of the stressed devices showed that, within the experimental uncertainty, their characteristics were not affected by either of the two stresses performed. This indicated that HTRB and HTGB stresses did not cause the measurable amounts of classic bias-temperature instabilities in the investigated devices.

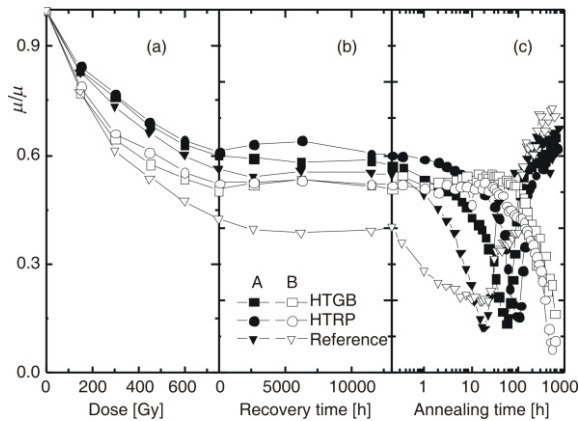
Devices from all groups were then irradiated at room temperature using a  $^{60}\text{Co}$  source at a dose rate of 0.13 Gy/s up to the total dose of 750 Gy(Si). After the irradiation, the devices were stored at room temperature for a year, with all terminals shorted, to recover spontaneously. Finally, the devices were annealed at 125 °C for 700 hours. During both irradiation and annealing, the gate bias was kept at 10 V, while the drain and source terminals were grounded.

Electrical characterization was done periodically by measuring the subthreshold and above-threshold transfer characteristics in saturation region using a PC-driven system of source measure units Keithley 237 and Keithley 2400.

The behaviour of  $V_T$  and  $\mu$  during the irradiation, recovery and annealing is shown in figs. 1 and 2. As can be seen, the irradiation caused a significant negative  $\Delta V_T$  and the reduction of  $\mu$  in all devices, the effects being more pronounced in the devices from the batch B. The larger  $\Delta V_T$  was observed in the pre-irradiation stressed samples, while the reduction of  $\mu$  was more considerable in the reference ones. Note that there was almost no difference between the radiation responses of HTRB and HTGB stressed VDMOSFETs from both batches. This is in line with



**Figure 1. Threshold voltage behaviour in power VDMOS transistors during (a) irradiation, (b) spontaneous recovery, and (c) annealing at 125 °C**



**Figure 2. Behaviour of channel carrier mobility in power VDMOS transistors during (a) irradiation, (b) spontaneous recovery, and (c) annealing at 125 °C**

an earlier finding that the radiation response appeared almost independent on the device pre-irradiation stress biasing for MOSFETs in different CMOS technologies [17]. Though,  $\Delta V_T$  and the reduction of  $\mu$  in our HTRB and HTGB stressed samples were slightly different (a slightly larger  $\Delta V_T$  in HTRB, and slightly larger reduction of  $\mu$  in HTGB stressed devices), which could be a consequence of different irradiation induced changes in  $N_{ot}$  and  $N_{it}$  densities. The results presented in [17] have shown similar behaviour of  $\Delta V_T$  in irradiated MOSFETs.

Figs. 1(b) and 2(b) show that the spontaneous recovery resulted in only a smaller increase of  $V_T$  and insignificant changes of  $\mu$ , the effects being somewhat more pronounced in the devices from the batch B. After the initial increase (within 3000 h),  $V_T$  remained almost constant in all samples except in the reference one from the batch B, fig. 1(b). In the devices from the batch A the initial increase of  $V_T$  was somewhat more pronounced in the stressed samples than in the reference ones, whereas in the devices from the batch B the initial increase was significantly lesser in the stressed samples. In the reference samples from the batch B, a significant initial increase of  $V_T$  was followed by somewhat less pronounced increase during the rest of the recovery time. As for the behaviour of  $\mu$  during the recovery, fig. 2(b), an insignificant increase followed by a negligible decrease in all stressed samples was observed. These changes were somewhat more pronounced in HTRB stressed samples from the batch A. On the other hand, in all reference samples, an initial decrease of  $\mu$  was followed by a slight increase.

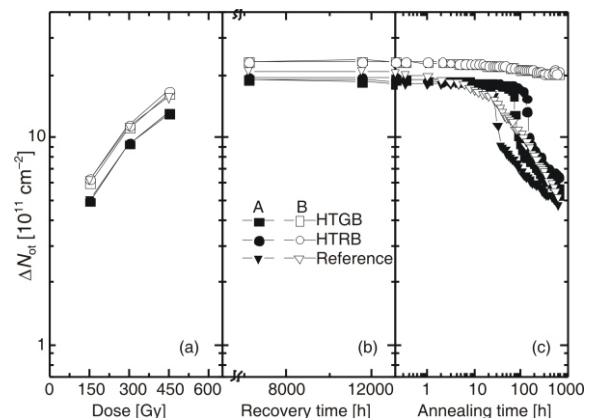
In contrast to the recovery, annealing at 125 °C had significant effects on both  $V_T$  and  $\mu$ , figs. 1(c) and 2(c). As can be seen, the changes of  $V_T$  and  $\mu$  appeared first in the reference samples. A slow increase of  $V_T$  in the early stage of annealing followed by a rapid increase was observed in all devices, except in the reference ones from the batch B, where the significant increase of  $V_T$  was observed from the very beginning of

annealing, fig. 1(c). A sudden rapid increase occurred first in the devices from the batch A, and then in those from the batch B. In contrast,  $\mu$  quickly decreased in all devices, fig. 2(c). The mobility reached its minimum after a certain annealing time, and then quickly increased up to the value somewhat higher than the one found after the irradiation. Figure 2(c) clearly shows that the minimum of  $\mu$  was achieved at first in all reference samples. In the case of the stressed samples, it appeared first in the devices from the batch A.

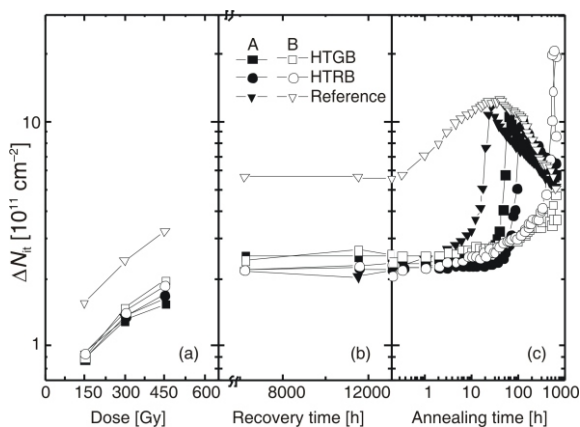
It should be noted that after the annealing time close to (but somewhat shorter than) the one corresponding to the mobility minimum,  $V_T$  begins to increase rapidly and quickly exceeds its pre-irradiation value. This phenomenon, known as the rebound effect [18], may cause device failures, thus leading to the faulty operation of the electronic system in which the devices are assembled. The rebound effect was observed in all devices from the batch A and in the unstressed samples from the batch B, and clear tendency to reach the rebound was observed in the stressed samples from the batch B, as well. Regarding the effects of pre-irradiation stressing, rebound occurred somewhat earlier in HTGB stressed samples from batch A, and almost at the same time in both HTRB and HTGB stressed ones from batch B.

## MECHANISMS RESPONSIBLE

The changes of  $V_T$  and  $\mu$  (figs. 1 and 2) are caused by underlying changes in the densities of  $N_{ot}$  and  $N_{it}$ . The behaviour of  $\Delta N_{ot}$  and  $\Delta N_{it}$  during irradiation, spontaneous recovery and annealing is shown in figs. 3 and 4, respectively. A subthreshold midgap (SMG) technique [10] was used to determine  $\Delta N_{ot}$  and  $\Delta N_{it}$ . The technique was not applicable after the irradiation at the highest irradiation dose levels (600 and 750 Gy(Si) because of the severe distortion of device



**Figure 3. Changes in the density of oxide trapped charge in power VDMOS transistors during (a) irradiation, (b) spontaneous recovery, and (c) annealing at 125 °C**



**Figure 4. Changes in the density of interface traps in power VDMOS transistors during (a) irradiation, (b) spontaneous recovery, and (c) annealing at 125 °C**

subthreshold characteristics, so these data are missing in figs. 3(a) and 4(a).

As can be seen in fig. 3, the behaviour of  $\Delta N_{ot}$  in both groups of transistors is qualitatively the same: it increases during the irradiation, saturates and remains nearly unchanged during the spontaneous recovery, and starts to decline only during the annealing. However, some important quantitative differences in  $\Delta N_{ot}$  between the devices with two different gate oxide thicknesses can be observed. Namely,  $\Delta N_{ot}$  is generally more pronounced in the devices with a 120 nm thick gate oxide than in 100 nm ones. Further, in the case of a thicker gate oxide, the effects of pre-irradiation burn-in stress can be observed already during irradiation, whereas in the case of a thinner oxide these effects are not observed during irradiation, remain rather insignificant during spontaneous recovery, and become considerable only after about twenty hours of annealing. In the case of the devices with the gate oxide thickness of 120 nm, it can be seen that: (1) irradiation causes a less significant increase of  $\Delta N_{ot}$  in the control samples than in the pre-irradiation burn-in stressed ones, (2)  $\Delta N_{ot}$  in the control samples during the spontaneous recovery saturates at a lower value than in the stressed ones, (3)  $\Delta N_{ot}$  during annealing decreases significantly in the control samples, but a rather small decrease is observed in the pre-irradiation stressed ones, and (4) HTRB and HTGB stress seem to have almost equal effects on  $\Delta N_{ot}$ . On the other hand, in the case of a 100 nm thick gate oxide, during irradiation there are no differences in  $\Delta N_{ot}$  behaviour between the control and pre-irradiation burn-in stressed samples. These differences remain insignificant during spontaneous recovery and even in the initial phase of annealing. After more than 20 hours of annealing  $\Delta N_{ot}$  begins to decline rapidly in all samples, but this decrease starts much earlier in the control samples than in the stressed ones, where the effects of HTGB stress are observed somewhat before the effects of HTRB stress.

Qualitatively similar behaviour of  $\Delta N_{it}$  in both groups of transistors is observed as well (fig. 4). Irradiation causes  $\Delta N_{it}$  increase in all samples, but a more pronounced increase is observed in the case of 120 nm gate oxide thickness. The increase of  $\Delta N_{it}$  is similar in all samples with the gate oxide of 100 nm, whereas in the case of 120 nm it is more pronounced in the control samples than in the burn-in stressed ones. Specifically, the radiation-induced  $\Delta N_{it}$  in the control samples with the gate oxide of 120 nm is about three times higher than in the other samples. During the spontaneous recovery,  $\Delta N_{it}$  in all samples remains almost constant as found after the irradiation. In the burn-in stressed samples,  $\Delta N_{it}$  in the devices with the gate oxide of 120 nm generally overlaps with corresponding  $\Delta N_{it}$  found in the 100 nm oxide devices, though the effects of HTGB stress seem stronger than the effects of HTRB stress for each thickness of the gate oxide. Finally, during annealing,  $\Delta N_{it}$  in the control samples with 120 nm oxide at first slowly increases, and after reaching the maximum begins to decrease. In all other samples, including both control and burn-in stressed devices with 100 nm oxide, as well as the burn-in stressed samples with 120 nm oxide, a sudden rapid increase of  $\Delta N_{it}$ , known as latent interface trap buildup (LITB) [19], is observed. The LITB occurs much earlier in the samples with 100 nm oxide (first in the control, and then in HTGB and HTRB stressed ones) than in 120 nm ones. Actually, the LITB in HTRB stressed samples with 120 nm thick oxide is several hundred hours delayed, but is more significant, so the corresponding  $\Delta N_{it}$  maximum is almost one order of magnitude higher than in the samples with 100 nm oxides. The delay of LITB in HTGB stressed samples is even larger, but clear tendency to attain a high maximum is observed as well.

As can be seen from figs. 3 and 4, most remarkable changes of  $\Delta N_{ot}$  and  $\Delta N_{it}$  occur during annealing, which is reflected in the changes of  $V_T$ , fig. 1(c), and  $\mu$ , fig. 2(c). This especially can be clearly seen in the samples with 100 nm oxide, where the slow decrease of  $\Delta N_{ot}$  and the increase of  $\Delta N_{it}$  in the early stage of annealing are in line with the slow increase of  $V_T$  observed in fig. 1(c), whereas the results shown in fig. 2(c) seem to be in accordance with the mobility degradation model [20], which implies that even small changes of  $\Delta N_{it}$  lead to the significant mobility decrease. The LITB process begins after the annealing time close to (but somewhat shorter than) the one that corresponds to the mobility minimum, whereas the slow decrease of  $\Delta N_{ot}$  continues.  $\Delta N_{it}$  reaches its maximum after the annealing time close to (but somewhat lower than) the one corresponding to the appearance of the rebound effect, and then starts to decrease. Approximately at the same time,  $\Delta N_{ot}$  starts also to decrease, but much faster.

Regarding the ionizing radiation, the knowledge acquired during many years of microelectronic devices testing [14, 21-23] has been successfully imple-

mented in explaining the impact of ionizing radiation on VDMOSFETs, and an appropriate model of responsible electrochemical process has been proposed in [8]. The essence of the model lies in an assumption that weak bonds between silicon and oxygen atoms in the oxide structure (as well as the bonds in the defects, between silicon atoms and hydrogen/hydroxyl groups and/or atomic clusters containing hydrogen) near the oxide-silicon interface are being broken upon irradiation. The results of this process are the appearance of unsaturated silicon atoms acting as hole traps (which form positive charge in the oxide), as well as hydroxyl groups or hydrogen related species, which are moving towards the interface by diffusion. Hydroxyl groups or other hydrogen related species can be also released in the process of defect dissociation initiated by hole trapping, which contributes to the buildup of  $N_{ot}$ . On the other hand, the creation of  $N_{it}$  is the consequence of breaking the weak atomic bonds at the oxide-semiconductor interface, either by holes or by diffused hydrogen related species.

It has been shown that thick gate oxides, unlike thinner oxides, contain many more strained atomic bonds, not only in the bulk, but also at the oxide-semiconductor interface [15]. As a result of the existence of numerous oxide and interface trap precursors, the stress induced buildup of  $\Delta N_{ot}$  and  $\Delta N_{it}$  is higher in thicker oxides, which leads to the significant degradation of device electrical parameters. This is confirmed by our results presented in figs. 3 and 4, as well. It can be clearly seen that  $\Delta N_{ot}$  and  $\Delta N_{it}$  are generally larger in the case of thicker gate oxides, not only during the irradiation, but also during the spontaneous recovery and annealing. Possible explanation for the pre-irradiation burn-in stress effects on  $\Delta N_{ot}$  and  $\Delta N_{it}$  behaviour during irradiation, proposed in our earlier paper [11], is that bias-temperature stress activates the metastable traps in the bulk oxide by releasing the hydrogen from previously passivated traps, thus increasing the probability of  $\Delta N_{ot}$  buildup. The diffusion of the released hydrogen species towards the interface leads to the passivation of interface trap precursors thereby reducing the probability of  $\Delta N_{it}$  buildup. Our earlier results [12, 13], as well as the results from fig. 3 in the current study paper, have clearly shown that there has not been any significant difference in the irradiation induced buildup of  $\Delta N_{ot}$  between the pre-irradiation stressed and the control samples. Therefore, it seems that the hydrogen species responsible for the passivation of interface trap precursors originate either from the package inside or from the layers adjacent to the gate oxide (polysilicon gate, CVD oxide, or passivation layer). The diffusion of these species towards the interface during burn-in stressing leads to the passivation of interface trap precursors, thus suppressing the radiation-induced buildup of  $\Delta N_{it}$  in the stressed samples (fig. 4).

During the spontaneous recovery, figs. 3(b) and 4(b), the radiation stress as a generator of new traps in the oxide and at the interface is disabled, and additional hydrogen particles are not created any longer. Consequently, the electrochemical processes of creating and passivating the oxide and interface traps, in which the hydrogen particles released during the irradiation participate, become balanced, so  $\Delta N_{ot}$  and  $\Delta N_{it}$  maintain almost constant values achieved at the end of the irradiation.

The behaviour of  $\Delta N_{ot}$  and  $\Delta N_{it}$  during annealing, figs. 3(c) and 4(c), can be satisfactorily explained by a model proposed hereafter, which similarly to some other models [24, 25] ascribes the leading role to  $H^+$  ions. The main difference between these models lies in the assumption about the origin of  $H^+$  ions. Our model is based on the assumption that in addition to  $H^+$  ions which were created during the formation of  $N_{ot}$  and  $N_{it}$  under irradiation, the  $H_2$  originating from the package inside and/or gate oxide adjacent layers is also present as a secondary source of  $H^+$  ions near the interface. An additional assumption is that hydrogen particles are more numerous in devices with thicker oxides. Thus, the  $H^+$  ions in these samples start electrochemical reactions at the interface as soon as the temperature is sufficiently increased, and are transformed into the atoms after picking up the electrons from the adjacent silicon. These H atoms may react with interface precursors and create interface traps, with  $H_2$  molecules being formed. The  $H_2$  molecules formed near the interface diffuse towards the oxide bulk and can be cracked at positively charged oxide traps, which leads to neutralisation of oxide trapped charge and to formation of  $H^+$  ions. The  $H^+$  ions drift under the positive oxide field towards the interface and the above reaction sequence is rounded up, resulting in a slight buildup of  $N_{it}$  in the early stage of annealing. The  $H^+$  ions, formed from the  $H_2$ , contribute to interface trap formation through the same reactions, but with delay, since the  $H_2$  slowly diffuse to the positions where the molecules are cracked. In the case of thinner oxide, the amount of  $H^+$  ions formed in the creation of  $N_{ot}$  and  $N_{it}$  traps under irradiation is significantly lower because of the lower concentration of weak atomic bonds and is obviously insufficient for initiating more electrochemical reactions with interface trap precursors in the early stage of annealing. That is why the leading role in annealing process must be attributed to delayed  $H^+$  ions originating from the  $H_2$  as the secondary source, which leads to the LITB activation. In pre-irradiation burn-in stressed samples, the sudden rapid increase of  $\Delta N_{it}$  is delayed due to the lower concentration of  $H_2$  available for cracking. Namely, some of the  $H_2$  have already been consumed for passivation of interface trap precursors during pre-irradiation burn-in stressing. The LITB delay in the samples with thicker oxide is more pronounced, and the most likely reason is the longer time required

for the diffusion of hydrogen particles from the package inside and structures adjacent to the gate oxide. In addition, the consumption of H<sub>2</sub> for passivation of interface trap precursors during the pre-irradiation burn-in stress is higher than in the case of thinner oxide. It should be noted that in devices with thicker oxides LITB is more pronounced as well.

## CONCLUSIONS

Different radiation, spontaneous recovery and annealing response, as well as different dependence on pre-irradiation burn-in stress, were found in power VDMOSFETs with different gate oxide thickness. The threshold voltage and carrier mobility dependences on pre-irradiation burn-in stress were less pronounced in devices with thinner gate oxides, which were clearly seen during irradiation and spontaneous recovery. Pre-irradiation burn-in stress caused delay in the changes of transistor electrical parameters during annealing, which was much more pronounced in devices with thicker gate oxide. The rebound of  $V_T$  and sharp minimum of  $\mu$  appeared later in the burn-in stressed samples than in the control ones for both groups of the investigated devices.

The main cause of the observed changes of electrical parameters were the changes in  $N_{ot}$  and  $N_{it}$  that were rather uniform during the irradiation and spontaneous recovery, but much more pronounced during the annealing in all samples. In the case of devices with thinner gate oxides, a sudden decrease of  $N_{ot}$  after 20 hours of annealing in the control samples was followed by similar behaviour of  $N_{ot}$  in the burn-in stressed samples, but with a pronounced delay. In the case of devices with thicker gate oxides, the decrease of  $N_{ot}$  has been more rapid in control samples, even in the initial annealing phase. As for the changes in  $N_{it}$  during annealing, LITB was observed in all devices with thinner gate oxides, and was only delayed in the burn-in stressed samples compared to the control ones. In the devices with thicker gate oxides, LITB was not observed in the control samples but only in the burn-in stressed ones, with an even larger delay.

The observed behaviour of  $N_{ot}$  and  $N_{it}$  has been explained by a model based on the assumption that H<sup>+</sup> ions, which have a key role in the relevant electrochemical processes, originate from two sources. A part is formed by breaking the weak atomic bonds during irradiation (these are activated immediately after the start of annealing, which in devices with thicker gate oxides causes an increase in  $N_{it}$  from the very beginning of annealing stage). The other H<sup>+</sup> ions are formed by cracking the H<sub>2</sub> molecules, which arrive from the package inside and structures adjacent to the gate oxide. During annealing, they drift to interface, causing LITB in all devices with thinner gate oxides, as well as in the burn-in stressed devices with thicker gate oxides.

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**ОДЖАРИВАЊЕ РАДИЈАЦИОНИХ ДЕФЕКТА КОД VDMOS  
ТРАНЗИСТОРА СНАГЕ СА УЛТРАДЕБЕЛИМ ОКСИДОМ ГЕЈТА  
КОЈИ СУ ПОДВРГНУТИ ТЕСТОВИМА ЖАРЕЊА**

У овом раду анализирано је оджаривање радијационих дефеката код VDMOS транзистора снаге са ултрадебелим оксидом гејта (100 nm и 120 nm), који су били подвргнути температурно-напонским тестовима жарења. У поређењу са фазом спонтаног опоравка претходно озрачених транзистора, показано је да су промене њихових електричних параметара (напон прага и покретљивости носилаца) током оджаривања проузроковане дејством повишене температуре и напона на гејту. Током оджаривања VDMOS транзистора снаге са оксидом гејта дебљине 100 nm, после почетног лаганог пораста, напон прага нагло почиње да расте достижући вредност већу од оне пре озрачивања. Код транзистора са оксидом гејта дебљине 120 nm, напон прага такође најпре лагано, а затим нагло (али са кашњењем) расте, са очигледном тенденцијом да се испољи поменути скок напона прага. Промене покретљивости носилаца током оджаривања су сличне код обе групе транзистора: покретљивост најпре лагано, а затим оштро опада, достиже минимум, а затим почиње да расте. У случају транзистора са дељим оксидом гејта ове промене су знатно спорије. Одговарајуће промене густина наелектрисања у оксиду и површинских стања анализирани су са аспекта одговорних механизма. Показано је да, код транзистора са дељим оксидом гејта, и промене густина наелектрисања у оксиду и површинских стања такође касне. Сви поменути феномени током оджаривања најпре су запажени код контролних узорака, а затим код узорака који су пре озрачивања изложени температурно-напонским тестовима жарења. Кључна улога у поменутим механизмима приписана је водониковим честицама.

*Кључне речи:* VDMOS транзистори, напон прага, покретљивост носилаца, наелектрисање у оксиду гејта, површинска стања, латентни пораст густине површинских стања, шесћиви жарења