THE METHODOLOGY FOR ACTIVE TESTING OF ELECTRONIC DEVICES UNDER THE RADIATIONS

by

***Aldo PARLATO*[1,2,3*], *Elio A. TOMARCHIO*[1], *Cristiano CALLIGARO*[2,4], *and Calogero PACE*[5]**

[1] Department of Energy, Information Engineering and Mathematical Models, University of Palermo, Palermo, Italy
[2] BlueCat Energy, Palermo, Italy
[3] Scientific Research Centre for the Economic Development and Industrial Innovation, Palermo, Italy
[4] RedCat Devices, Milano, Italy
[5] Department of Information Engineering, University of Calabria, Rende, Italy

Scientific paper
http://doi.org/10.2298/NTRP1801053P

The methodology, developed for active testing of electronic devices under the radiations, is presented. The test set-up includes a gamma-ray facility, the hardware board/fixtures and the software tools purposely designed and realized. The methodology is so wide-ranging to allow us the verification of different classes of electronic devices, even if only application examples for static random access memory modules are reported.

Key words: testing methodology, electronic device, total ionizing dose, single event effect, gamma ray

INTRODUCTION

Technologically-enhanced electronic devices are used in various fields such as the accelerator-based facilities, nuclear power plants, space mission applications, avionics, and so on. This kind of devices can be exposed to the intense radiation over time which may impair the functioning of the equipment. The failures induced by the radiation are one of the most challenging issues for modern electronic systems, in particular for space applications where the reliability is the concern [1, 2]. Many efforts have been spent in the last decades to measure, model, test and mitigate the radiation effects, applying numerous different techniques approaching the problem at various levels [3].

The radiation effects in electrical, electronic, and electromechanical (EEE) components can be separated into cumulative effects, which lead to a progressive degradation of the component characteristics, and the single event effects (SEE), which gather destructive or non-destructive types of events.

The cumulative effects include both the total ionizing dose (TID) and the displacement damage (DD), also called the total non-ionizing dose (TNID). The TID effects are induced by the transfer of the ionising energy from the radiation exposure, which thermalized in the creation of the electron-hole pairs in the component material. These charges typically get trapped in the dielectric layers (*e. g*. oxides or nitrides) either in the bulk of the dielectric, or in the proximity of the interface with the semiconductor, where the electrostatic effect on the device operation is maximum. This produces a variety of effects on the device characteristics such as the flatband and the threshold voltage shifts, leakage currents and timing skews [3].

The TNID effects are induced by the non-ionising transfer of energy, *i. e*., by the interaction of primary and secondary energetic particles with component atoms, and eventually creating the damage and stable electrically active defects in the semiconductor crystal lattice.

The SEE is caused by the same fundamental mechanism: the collection of charge at a sensitive region of a microcircuit following the passage of an energetic particle through the device [4]. Some of them, such as the single-event transient (SET), single-event upset (SEU) and single-event functional interrupt (SEFI) are temporary and can be recovered. Others can lead to a permanent damage such as the single-event latch-up (SEL) or single-event gate rupture (SEGR).

The requirements on TID and SEE depend on the final application of the device and can be very different. For example, for space applications, the re-

* Corresponding author; e-mail: aldo.parlato@unipa.it

ceived TID on Silicon (Si) typically ranges from few krads (Si) to several 100 krads (Si), depending on the spacecraft mission, orbit, and device shielding [5, 6]. For device used in the interplanetary mission, in the high-energy physics experiments, the TID ranges from few Mrad* (Si) to several Mrad (Si) [7].

Usually, the electronic components to be tested are designed to be radiation resistant but the control electronics can be a commercial type or only rad-tolerant. This implies a damage problem on the test control electronics and an uncertain degree in the test itself as it could be difficult to discriminate the component or system failure in the case of error.

It follows that it is very important to develop the irradiation methodologies and realize test facilities which can simulate the different radiation conditions, the kind of operations and the intrinsic nature of signals (analog or digital), to which electronic devices may be subject. A general-purpose testing solution does not exist yet off-the-shelf, thus custom methods and technologies for testing electronic devices have been developed.

The aim of this work is to describe the testing methodology besides the realized boards/fixtures, customized for different electronic devices, developed and tested by using the gamma irradiation facility of the University of Palermo. Considering the wide scenario of electronic components used for space applications, in this paper we will focus our attention on static random access memories (SRAM). The SRAM are considered one of the most critical components since they can be found either as the stand-alone device on payloads or as embedded memories in more complex application specific integrated circuits (ASIC), such as the microcontrollers, core processors or digital signal processing (DSP). Typical errors affecting SRAM are the SEL, the SEGR and a very wide spectrum of soft errors spreading from the SEU to the multiple bit upset (MBU), the SEFI and, more in general, the cumulative soft error gathered in the matrix array for a long time.

In this work, the rad-hard components from the RedCat Devices have been used. More specifically: RC7C512RHS (512 kbit SRAM for space applications), RC7C512RHH (512 kbit SRAM for high energy physics), RC7C512RHM (512 kbit SRAM from low orbit applications) and RC7C1024RHS (1 Mbit SRAM for space applications) having the resistance from 300 krad (Si) for RC7C512RHM up to 25 Mrad (Si) for RC7C512RHH and the immunity to SEL for all the components up to 80 MeVcm^{2}mg^{-1} (Si).

THE GAMMA IRRADIATION FACILITY

The gamma irradiation facility of the University of Palermo is a research facility which replicates, in reduced scale, the industrial installations and provides a good versatility to perform different types of irradiations. The overall irradiation equipment consists of an irradiation cell, the gamma irradiator "Irradiatore Gamma Sicilia-3" (IGS-3) and an external control room.

*1 rad = 10^{-2} Gy

Figure 1. The photo of the IGS-3 gamma irradiator

The IGS-3 gamma irradiator (see fig. 1) is actually equipped with a total of 4.31 TBq ^{60}Co gamma ray sources.

It is composed of 12 cylindrically shaped sources featuring different activities: 6 sources of 0.13 TBq each, 3 sources of 0.24 TBq each, and 3 sources of 1.26 TBq each [8]. The facility is fully equipped with the instrumentation for the dosimetry, in order to ensure safe operations and radiation levels according to the international standards ESCC No. 22900 [9].

Inside the irradiation cell, we can distinguish two areas: an area with a direct exposure to radioactive sources, which we might call the "hot room", and a shielded area from radioactive sources which we might call the "warm room". In the hot room, the radiation fields are very high and the safety systems do not allow anyone to access during the irradiation. It is also inadvisable to place any electronic equipment or other device if not properly shielded because, after a short time, they would be severely damaged. In the warm room, the radiation fields are weaker and it is possible to place the equipment and the control instrumentations. The control panel is placed outside the irradiation cell, in a fully shielded room (the "control room"), where a safe access is allowed.

Considering these severe environment conditions, it is clear that a new testing strategy shall be de-

fined. The usual measurements layout, typically performed using the test board where the device under test (DUT) is mounted and a lab setup with the equipment suitable to generate waveforms and collect the outputs, is not viable. Only the DUT shall be exposed, while the measurement equipment and the auxiliary active circuitry cannot be placed under or close to the irradiation beams. A remote control of all measurement operations is mandatory.

THE TEST METHODOLOGY DEVELOPMENT

The presence of different working areas with different access modes and radiation levels makes the preparation of the irradiation testing of electronic devices working in active mode difficult. Indeed, it is necessary to provide the power (with the power supply systems) and to monitor the component performances (with instrumentations), but it is recommended to place the control equipment at least in the warm room, in order to avoid that probable failures of control devices could affect the experiment or lead to false results.

This arrangement is not always possible since the power supply system, the auxiliary circuitry and the monitor devices must often be a complementary part of the DUT and they shall be placed nearby.

In this case, it is also mandatory to provide the appropriate shielding that enables both the reduction of the radiation dose rate in sensitive areas and the connection of such equipment with the outside. This means the shielding part of the equipment and arranging the appropriate connection cables in order to avoid the "radiation drafts" in the shielded area. At the same time, the experiment arrangement must be designed to be operated completely from the outside (in the control room), without any need to intervent into the irradiation cell, since this would imply the recovery of the sources and the halt of the test. Also, it must be realized taking into account the ESCC Basic Specification No. 22900 [9] and the MIL-STD-883H Method 1019.8 [10].

This target has been achieved by ensuring the precise positioning of DUT and realizing the connections step by step through the various rooms (the hot room, the warm room, the control room). The proposed solution is based on splitting the test board in:

– the mother-board (MB) which hosts the signal generator, the data acquisition system and the auxiliary circuitry, and
– the daughter-board (DB) with the DUT only.

The DB with DUT is connected with flat cables to the MB which hosts the control electronics. The flat cable is certainly a critical element which, in a common testing, is not used because it can introduce the delays in the communication between the MB and the DB. Fortunately, up to now, the electronic components for space applications do not work at very high frequencies, because the design choices taken to make them rad-tolerant (or rad-hard) usually limit the working frequency. More specifically, focussing this work on SRAM, edge-less shaped transistors used to mitigate the charge trapping and the enhanced guard rings to avoid SEL, in regions where the *n*-channel and the p-channel transistors are close to each other, require a layout design far from the minimum guaranteed by the technology. This means that the internal logics cannot switch at the maximum frequency, thus leading to the access time below 10 ns for those components having a TID around 300 krad (Si) and over 12 ns for those having a TID up to 25 Mrad (Si). These frequencies are typical for standard payloads running core processor (*e. g*. Cobham Aeroflex LEON) able to run up to 50 MHz (20 ns) and of course are quite far from the commercial SRAM running in standard processors running up to 120 MHz (8.3 ns). Therefore, the critical element such as the 52-poles flat cable can be still acceptable, provided that its length does not exceed the maximum of half a meter and can run without the significative degradation frequency in the range of 50 MHz. Over this length, a different cable must be taken into account or the test should be carried out at lower frequency (*e. g*. 25 MHz). For analog signals, such as those fed as the input to data converters, coaxial cables shall be adopted but of course a reduced number of pins can be driven.

Both MB and DB design shall be accurate. In its simplest version, the MB hosts a field programmable gate array (FPGA, Xilinx Spartan-3) that generates all waveforms needed for the DUT, performs the output data acquisition, controls the system and the interfaces to the laptop by the means of an USB (fig. 2). This arrangement is suitable, for example, for testing the rad-hard memories [11-13].

A more sophisticated version has also a simple power generation circuit on-board, in order to provide the needed supplies through flat cable to the DUT, without any external electronic supplies.

If required by the test, the MB can also have more complex auxiliary circuitry on-board to generate the reference analog signals and to provide all necessary inputs/outputs for the testing of analog rad-hard components, such as the data converters and power MOSFETS. In this case, the additional flat cable and coaxial cables connect the two boards.

The DB design, although simple, must be also accurate. On it, neither active components (such as the microcontrollers, microprocessors, level-shifters, *etc*.) nor passive sensitive components (electrolytic capacitors, resistors, inductors, *etc*.) can be mounted, as their degradation could affect the test results.

Both boards layout must be optimized, with a respect to the ground and the power supply planes, in order to guarantee most stable as possible the working

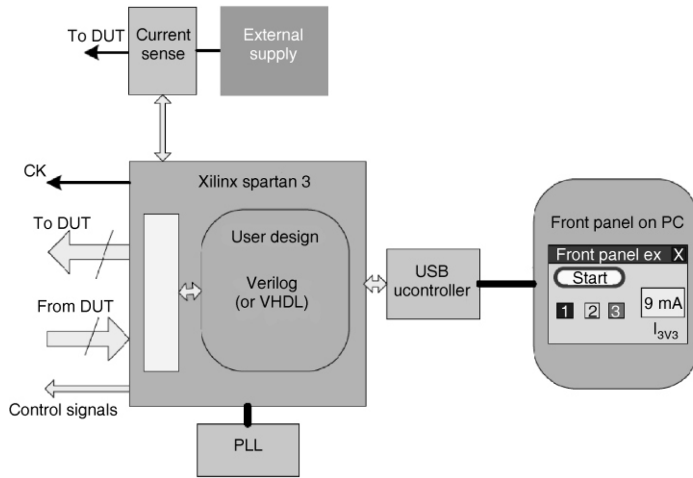

Figure 2. The mother-board simplified block diagram

boundary conditions. The degradation from above mentioned components used to drive DB becomes evident starting from 5 krad (Si) and for the microcontroller and the microprocessor is mainly due to SEFI (the controller must be rebooted very frequently). The level-shifter may have a wrong translation of voltage leading so to the lower driving address and control signals while passive components (capacitors, resistors and inductors) can show a voltage shift. Above 5 krad (Si) active components usually fail (including the FPGA) thus leading to the impossibility to continue the experiment. Considering that the DUT must be resilient up to 300 krad (Si) or, for more resilient components, up to 25 Mrad (Si) it is mandatory to have a good protection strategy for MB in order to avoid the failure and do not affect the results of the exposure on DB.

As an example, fig. 3 shows the two boards and main connections for the test of the 1Mbit asynchronous rad-hard SRAM (RC7C1024RHS, 128 kbit x8) memory device, using the six transistor (6T) memory cell SEU-enhanced with Miller capacitors [11]. It has been integrated in a 180 nm standard CMOS process with a dedicated rad-hard-by-design (RHBD) approach using edge-less transistors (ELT) and enhanced guard-rings. The DB communicates via flat cable with the MB, but all the power supplies are independent. So, in this case, it is necessary to provide a stabilized external power supply that does not bring any noise to the DUT. This latter is hosted in a zero insertion force (ZIF) socket in order to give a mechanical stability to the overall structure. The whole DB can be considered passive, with the DUT as the only active element which will be the only target of the incident radiation.

In fig. 4, the precise positioning of the above described experimental set-up within the "hot room" of Gamma facility is shown.

The MB is shielded by means of lead bricks. However, although MB is the most sensible element to be protected during the irradiation, we must consider that it needs to communicate with a personal computer in order to allow the operator to control the experiment. The low dose rate on the DB (0.012 Gys^{-1}) and the radiation attenuation at a value of about one hundred times lower on the shielded MB ensures the survival of the equipment.

The same approach can be used also for the testing under heavy ions and protons. For heavy ions, there are not any major concerns related to the TID since this kind of tests are limited in time (*e. g.* 20 minutes to reach 60 $MeVcm^2mg^{-1}$ (Si) using Xe ions for

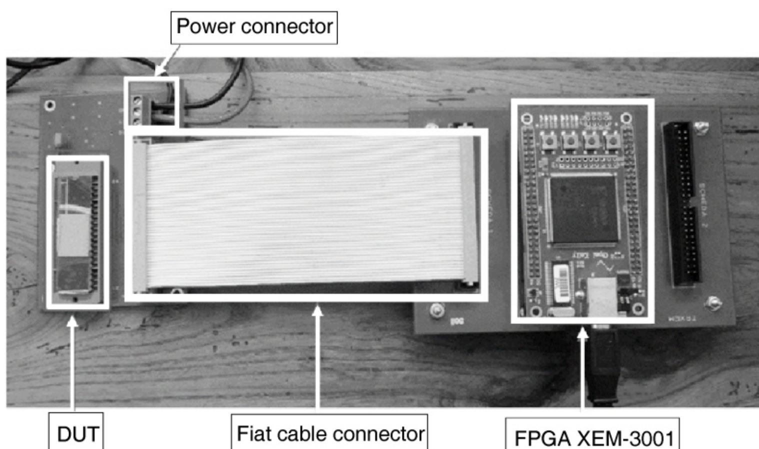

Figure 3. The photo of MB (right) and DB (left) and the relevant connection

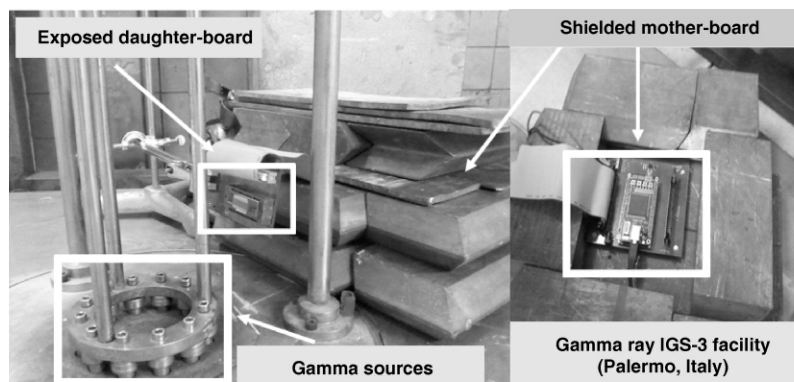

Figure 4. The placement in the hot room of MB (protected) and DB (exposed)

SEL) and do not provide any trapping in the silicon dioxide (direct ionization); for protons, the only risk is to have the activation of the board as the result of spallation effects coming from the interaction with the glass passivated chips used to protect the components and usually having borophosposilicate glass (BPSG). In both cases, a good protection of MB is recommended to avoid the SEE for heavy ions and the activation for protons.

The connections between the hot and the warm rooms were realized through the USB connection, while between the warm and the control rooms were realized through the coaxial or Ethernet cable. All the equipment within the warm room is remotely managed from the control room.

The remote control of the entire test session was carried out realizing a virtual private network (VPN), able to connect the control room by means of an appropriate commercial software (VNC server, TeamViewer, *etc*.) enabling an external network connection. A basic VPN configuration was carried out and successfully tested with multiple connections from Milan (RedCat Devices) and Cosenza (DIMES) to the control room of Palermo.

Regarding software tools, a Verilog code has been written in order to generate all the functions that shall be provided by FPGA. Moreover, a suitable interface has been developed in Visual Basic to control all the operations from the laptop through the USB. The control is based on the interface (Opal Kelly's FrontPanel^{TM}) that handles all the interactions between the virtual controls and the FPGA internals.

The memory test allows us to apply a very different pattern such as the checkerboard, the negate checkerboard, the March and other more complex tests and evaluate the number of bit failure coming from the degradation of the memory array. This operation is carried out during the irradiation and controlled by the automatic procedures (software routines) or directly by testing the engineers connected to the board.

Figure 5 summarizes the methodological approach of the above-described technological test environment.

The testing solution shown in fig. 5 allows a significant degree of flexibility and easiness in the preparation of the experiment. The flexibility and the effectiveness of the experimental set-up have been successfully tested in other irradiation facilities with different lay-out, sources and kind of tests (the TID or the SEE), using the same methodology. A set of test irradiations were performed using the heavy ions at radiation effects facility (RADEF), Jyvaskyla University, Finland, and protons at the svedberg laboratory (TSL), Uppsala University, Sweden. At RADEF, several ions have been used in order to test the soft and the hard errors with linear energy transfer (LET) going from 4-5 MeVcm^{2}mg^{-1} (Si) up to 60 MeVcm^{2}mg^{-1}.

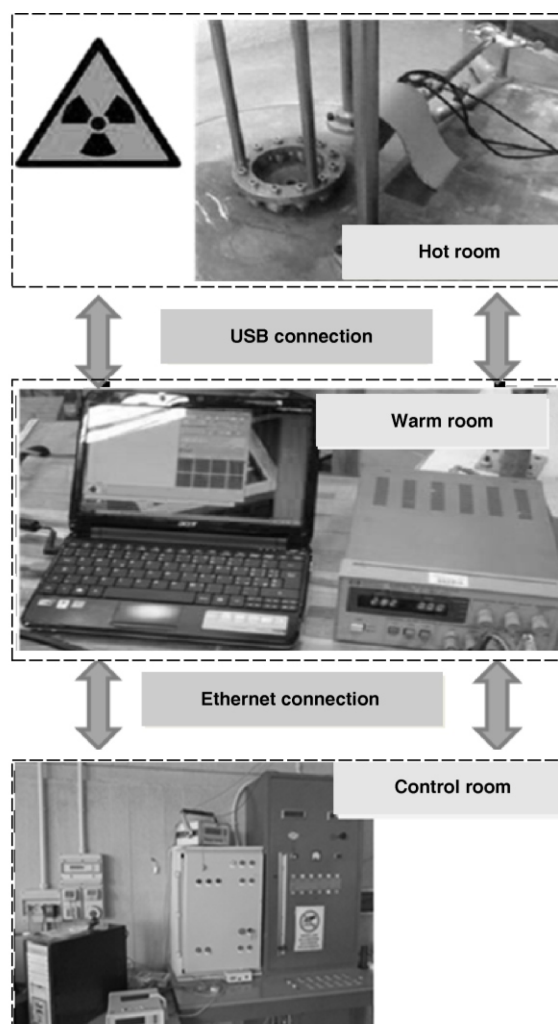

Figure 5. The logical split of environments and hardware connections

Table 1. Main parameters measured (MEAS) directly from the beam for heavy ions irradiation tests and comparison with ones simulated from the stopping and range of ions in matter (SRIM)

Ion	Energy [MeV]	LETMEAS at surface [MeV $mg^{-1}cm^2$]	LETMEAS at Bragg peak [MeV $mg^{-1}cm^2$]	LETSRIM at surface [MeV $mg^{-1}cm^2$]	LETSRIM at Bragg peak [MeV $mg^{-1}cm^2$]	RangeSRIM [microns]
$^{15}N^{+4}$	139	1.87	5.92 (at 191 m)	1.83	5.9(at 198 m)	202
$^{20}Ne^{+6}$	186	3.59	9.41 (at 138 m)	3.63	9.0 (at 139 m)	146
$^{30}Si^{+8}$	278	6.53	13.7 (at 114 m)	6.40	14.0 (at 120 m)	130
$^{40}Ar^{+12}$	372	10.07	18.9 (at 100 m)	10.2	19.6 (at 105 m)	118
$^{56}Fe^{+15}$	523	18.59	29.7 (at 75 m)	18.5	29.3(at 77 m)	97
$^{82}Kr^{+22}$	768	31.21	41.7 (at 68 m)	32.2	41.0 (at 69 m)	94
$^{131}Xe^{+35}$	1217	57.36	67.9 (at 57 m)	60.0	69.2 (at 48 m)	89

With reference to the example of layout experiment carried out with heavy ions at RADEF facility showed in fig. 6, the LET values measured (MEAS) directly from the beam and obtained as a simulation from the Stopping and the Range of Ions in Matter (SRIM) are summarized in tab. 1.

At TSL the protons beam with energy up to 180 MeV has been used mainly for soft errors test. The fluency obtained has been 3.9 10^{11} cm^{-2}. Each test was realized following the ESCC Basic Specification No. 25100 [14]. Figure 7 shows the layout of the experiment performed with protons at TLS Laboratory.

All the testing was successfully performed. Only during the test under protons, the DB highlighted some traces of activation due to the presence of gold traces in the socket ZIF and in the power supply; however,

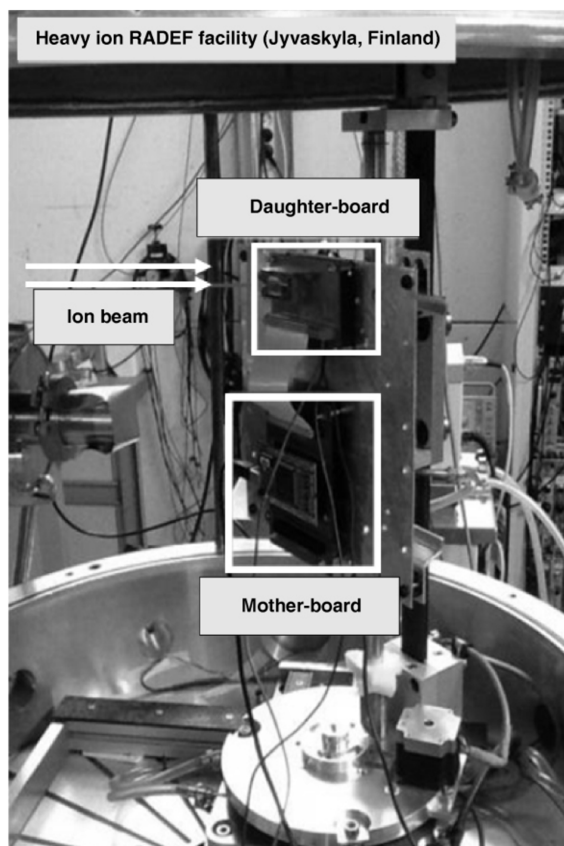

Figure 6. The testing set-up in heavy ions irradiation facility in Jyvaskyla (Finland)

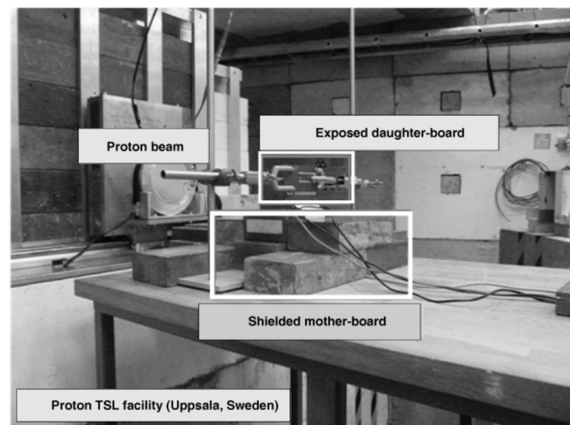

Figure 7. The testing set-up in protons irradiation facility in Uppsala (Sweden)

such activation is not relevant from the radiation protection point of view and did not affect the outcome of the tests or upset the results. No test under the neutrons have been done by using this equipment.

CONCLUSIONS

The developed test methodology has proved effective and allows a significant degree of flexibility associated with the easiness in the preparation of the test experiment, making a powerful tool for the test of rad-hard components under radiations available. Therefore, the same test methodology and the technology can be performed with different kind of test (the TID and the SEE) and different radioactive sources (gamma ray, protons and heavy ions). In fact, the test methodology, initially developed for the TID test under the gamma radiation (^{60}Co sources), has been successfully carried out for the SEE test with protons and heavy ions.

Different test-boards and software tools have already been developed and assessed for the testing of data converters [15] and power MOSFET, even if only application examples for SRAM) modules are reported. Due to the flexibility of the proposed lay-out, the testing methodology can be extended to other classes of components, such as the microprocessors, bandgap references, phase-locked loop (PLL), and so on.

The authors consider particularly promising the possibility, thanks to this approach, to make tests in very low dose rate regime. Such tests usually require long time frames (up to months) not necessarily with ^{60}Co but using different means of source (*e. g.* ^{241}Am). Very low dose rate tests are particularly suitable to reproduce space conditions on Earth and thanks to a fully automatic test with periodical remote check can be a cost effective solution for space components qualification.

As a final remark it is worth to underline how this methodology shows its main advantage in the in-situ approach giving researchers a very powerful tool for making different tests at component level during the irradiation sessions. This means an increased flexibility at a lower cost per session considering that the component must not be removed from the irradiation chamber and tested in a different (and protected) environment.

ACKNOWLEDGEMENT

This work has been partially supported by the Italian Ministry of Foreign Affairs inside the Italy-Israel Cooperation Programme (ATENA Project).

AUTHORS' CONTRIBUTIONS

The test methodology was carried out by A. Parlato, C. Calligaro, and C. Pace. The gamma ray test experiments were performed by A. Parlato and E. A. Tomarchio, whereas the heavy ion and proton tests were carried out by C. Calligaro and C. Pace. All authors analysed and discussed the results. The manuscript was written by A. Parlato, C. Calligaro, C. Pace and E. A. Tomarchio. The figures were prepared by A. Parlato and E. A. Tomarchio.

REFERENCES

[1] Cappello, S. G., *et al*., Gamma-Ray Irradiation Tests of CMOS Sensors Used in Imaging Techniques, *Nucl Technol Radiat, 29* (2014), Suppl., pp. S14-S19

[2] Consentino, G., *et al*., Dangerous Effects Induced on Power MOSFET by Terrestrial Neutrons: A Theoretical Study and an Empirical Approach Based on Accelerated Experimental Analysis (2013) AEIT Annual Conference: Innovation and Scientific and Technical Culture for Development, AEIT 2013, Mondello, Palermo, Italy

[3] ***, European Cooperation for Space Standardization,ECSS-Q-HB-60-02A Techniques for Radiation Effects Mitigation in ASIC and FPGA Handbook, 1 September 2016

[4] ***, IEEE Nuclear and Space Radiation Effects Conference, Short Course on Radiation Effects in the Space Telecom Environment, July 12, 1999

[5] Mavis, D. G., Alexander D. R., Employing Radiation Hardness by Design Techniques with Commercial Integrated Circuit Processes, *Digital Avionics Systems Conference, 1* (1997), Oct., pp. 15-22

[6] Clark, L., *et al*., Optimizing Radiation Hard by Design SRAM Cells, *IEEE Trans. on Nucl. Sc., 54* (2007), 6, pp. 2028-2036

[7] Haddad, N. F., *et al*., Incremental Enhancement to SEU Hardened 90 nm CMOS Memory Cell, *Proceedings*, 11th Europ. Conf. on Radiation and its Effects on Components and Systems (RADECS 2010), Aqua Dome Langenfeld, Austria, September 20-24, 2010

[8] Fiore, D., *et al*., The DEIM Irradiation Facilities for the Testing of RAD-HARD Components (in Italian), Italy, 2015

[9] ***, Total Dose Steady-State Irradiation Test Method, ESCC Basic Specification n. 22900, Issue 4, 2010

[10] ***, MIL-STD-883H, Method 1019.8, Ionizing Radiation (Total Dose) Test Procedure, 2010

[11] Calligaro, C., *et al*., A 15 Mrad(Si) 512 Kbit Rad-Hard SRAM in a Standard 0.18 m CMOS Technology, *Proceedings*, 13th Europ. Conf. on Radiation and its Effects on Components and Systems (RADECS 2012), Biarritz, France, September 24-28, 2012

[12] Arbat, A., *et al*., Radiation Hardened 2M bit SRAM in 180 nm CMOS Technology, IEEE-AESS Conference in Europe about Space and Satellite Telecommunication 2012 (ESTEL), November 2012

[13] Calligaro, C., *et al*., A Multi-Megarad, Radiation Hardened by Design 512 kbit SRAM in CMOS Technology, 22nd International Conference on Microelectronics (ICM2010), Il Cairo (Egypt), Dec., 2010, pp. 375-378

[14] ***, Single Event Effect test Method and Guidelines, ESCC Basic Specification No. 25100, Issue 2, 2014

[15] Mahoney, M., DSP Based Testing of Analog and Mixed-Signal Circuits, Wiley IEEE Computer Society, 1987

Received on June 16, 2107
Accepted on January 29, 2018

Алдо ПАРЛАТО, Елио А. ТОМАРКИО, Кристијано КАЛИГАРО, Калођеро ПАЧЕ

МЕТОДОЛОГИЈА АКТИВНОГ ТЕСТИРАЊА ЕЛЕКТРОНСКИХ УРЕЂАЈА ИЗЛОЖЕНИХ ЈОНИЗУЈУЋИМ ЗРАЧЕЊИМА

Приказана је методологија развијена за потребе активног тестирања електронских уређаја при излагању јонизујућем зрачењу. Поставка за тестирање садржи наменски осмишљено и реализовано постројење са извором гама зрачења, експерименталну апаратуру и пратеће алате у виду програмских пакета. Методологија има тако широку примену да омогућава тестирање различитих класа електронских уређаја, мада је приказана само примена за модуле статичке меморије са насумичним приступом.

Кључне речи: методологија тестирања, електронски уређај, укупна доза јонизације, ефекат појединачног догађаја, гама зрачење